ABSTRACT OF THE DISCLOSURE

In one embodiment of the present invention, a bus controller is used in a multi-master system having first and second processors. The bus controller includes a bus arbiter and a first multiplexer. The bus arbiter is coupled to the first and second processors via first and second master buses, respectively, to generate an arbitration select signal based on result of arbitrating bus access information from the first and second processors. The first multiplexer is coupled to the first and second master buses and a first slave bus in a plurality of slave buses to provide device access information selected from the bus access information using the arbitration select signal. The device access information is transferred to a first slave device connected to the first slave bus.